VERY LINEAR X-BAND MIC BIPOLAR VCO WITH 100MHz FM RATE

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Abstract

This paper describes a microstrip, doubling mode bipolar transistor oscillator (osciplier), varactor tunable over 8-10GHz with an output power of 12dBm±1dB. It has an FM rate of 100MHz with a set-on accuracy of ±8MHz from perfect linearity (i.e. ±0.1%) and frequency pulling ±1MHz into a 2:1 mismatched load. Power flatness and frequency pulling immunity is achieved using a two stage GaAs FET buffer/limiter. It maintains these specifications over a temperature range of -54°C to 100°C.

Introduction

Previously, fundamental mode bipolar transistor VCOs have been made using hyperabrupt junction varactors[1]. They were purported to be the ultimate solution for high linearity. Unfortunately, even if extensive diode selection is undertaken, a typical unlinearized hyperabrupt varactor oscillation has a linearity in X-band which is no better than ±30MHz. Consequently, for linearity < ±10MHz linearizers have to be incorporated, rendering them no improvement over abrupt junction devices. In fact, from an output power standpoint, hyperabrupt varactors are at least 3dB worse than abrupt varactors. Furthermore, designs using a single bipolar transistor operating at the fundamental frequency in X-band[2] suffer significantly in terms of frequency pulling compared to an osciplier whose transistors are each operating fundamentally at half the output frequency and the varactors provide not only tuning but frequency doubling.

Gunn oscillators require too large a tuning voltage range, limiting slew rate and FET oscillators often suffer from stability problems, as well as a tuning range too large for many ECM systems[3].

The Sub-System

VCO frequency characteristics are heavily dependent on temperature. This problem was eradicated by maintaining the complete sub-system (Fig. 1) at a temperature of 80°C±1°C by a miniaturised proportionally controlled thermoelectric heater/cooler. Frequency pushing was eliminated by regulating the transistor power supplies to 12±0.01V. Fig. 1 illustrates the MIC VCO output into an attenuator then through a buffer/limiter. The command voltage to the VCO is via a buffer amplifier and linearizer.

MIC VCO

The circuit diagram of Fig. 2 is a classic oscillator whose fundamental is generated by each transistor then doubled by the varactors. Incidentally, the SRD provides the most efficient doubling, but its doping profile reduces its $\delta C/\delta V$ characteristic compared to a varactor. This increases the V-f non-linearity which reduces the modulation sensitivity. The conditions for oscillation were facilitated by a computer-aided nodal analysis using small signal S parameters for the transistors used. The ingenuity with this simple circuit was in translating it to a microstrip form (on alumina) without introducing parasitics which perturb the fine grain linearity. This was achieved by using lumped inductors for the bias lines into the active devices and lumped MOS chip capacitors wherever possible. Thin-film tantalum nitride resistors were used for bias resistors. Sub-pf pads were strategically placed to be bonded in to account for disparities in the device characteristics from one half of the circuit to the other. Perfect balance is essential. Long term PTD is eliminated by using diodes oxide/nitride passivated and good heat sinking of all active devices.

Having obtained a f-V curve (Fig. 3) which almost overlaps the C-V curve, a low capacitance diode breakpoint linearization restores the non-linear curve to a very high degree of linearity (±0.1%). In order to achieve this without the loss of video bandwidth, the bias to the varactors from the linearizer must be via a singly terminated low pass filter. Interfacing the linearizer with the VCO frequency command signal necessitates a 100MHz buffer amplifier.

Buffer/Limiter

A frequency pulling immunity of < ±1MHz is achieved by providing the VCO with >45dB of load isolation. A 2-stage balanced GaAs FET amplifier was designed to give a minimum of 10dB of gain and an S_{12} >35dB across the band of interest. The remaining 10dB was realized by incorporating a 6dB Ta_2N thin film π attenuator (i.e. 12dB isolation) at the output on the oscillator substrate. The output power from the oscillator was adjusted to allow the minimum power to saturate the amplifier. By this means, for example, a 6dB variation of oscillator output power would be compressed to < 1dB provided the minimum power level is sufficient for saturation. The saturated output power of an FET typically drops at 1.5dB/octave. A broadband amplifier (5-10GHz) was designed to incorporate other VCOs within the same subsystem. Its performance is shown in Fig. 4.

Discussion of Results

1. The linearity of ±8MHz (Fig. 5) is a conservative figure, and values of ±5MHz have been seen in 'laboratory prototypes'. The linearity limitation is the fine grain modulation sensitivity variation caused by circuit parasitics. These could be accounted for, and the linearity still further improved, by increasing the number of break points in the linearizer, but at the expense of reduced slew rate (or FM rate). As the number of break points increases, so does the rise time of a pulse through the RC linearizer network.

2. The frequency pulling immunity was < ±1MHz into a 2:1 load. The FET amplifier served its purpose with an increase in cost compared to a 4 port isolator, but had the added advantage of providing flat output power and smaller size.

3. PTD in range 1ms - 1s was rather high at ±3MHz, but this can be improved by using a BeO substrate for the heart of the VCO. The short term PTD (10ns - 1ms) was ± 5MHz.

4. The VCO was found to be capable of being modulated from 8 to 10GHz at the rate of 100MHz.

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References

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3. Tserng, H.Q. and Macksey, H.M., Wide-Band Varactor-Tuned GaAs MESFET Oscillators at X- and Ku-Bands, p.267-8, 1977 IEEE MTT-S International Microwave Symposium Digest.

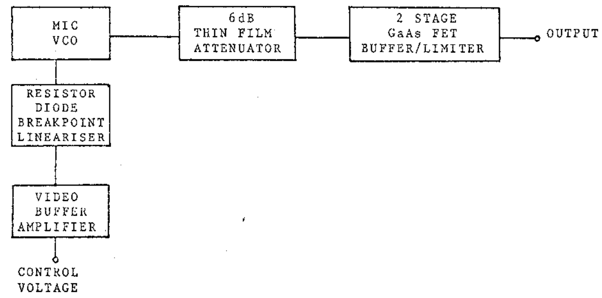

FIG. 1 THE SUBSYSTEM SCHEMATIC

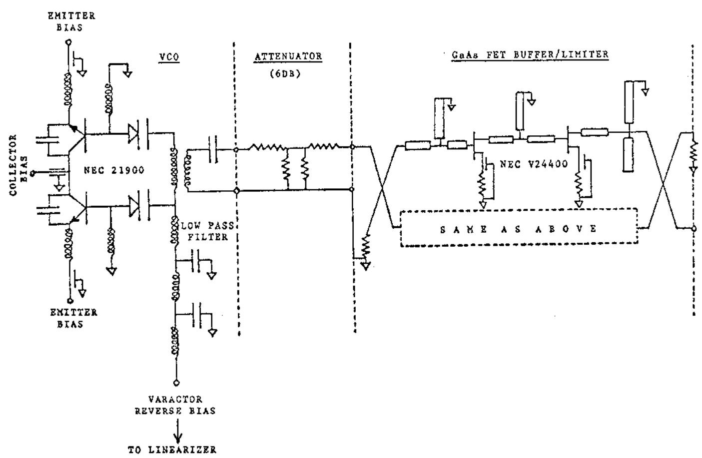

FIG. 2 THE RF CIRCUIT

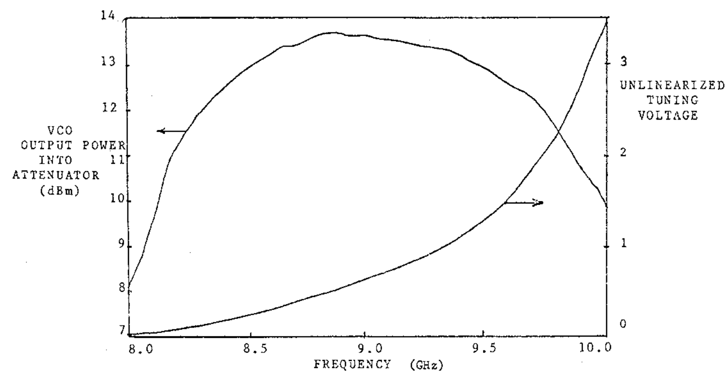

FIG. 3 FREQUENCY VS. UNLINEARIZED TUNING VOLTAGE AND POWER

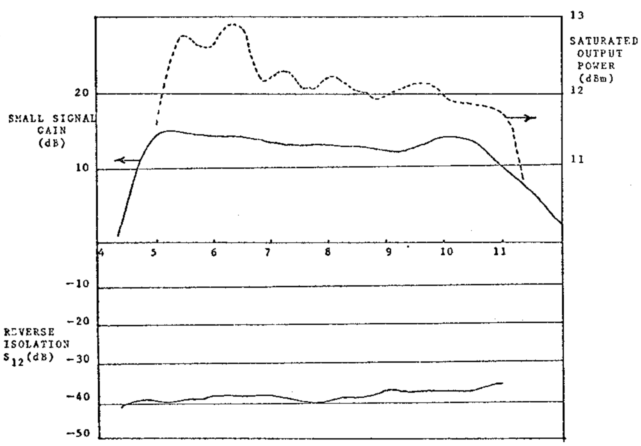

FIG. 4 BUFFER/LIMITER PERFORMANCE

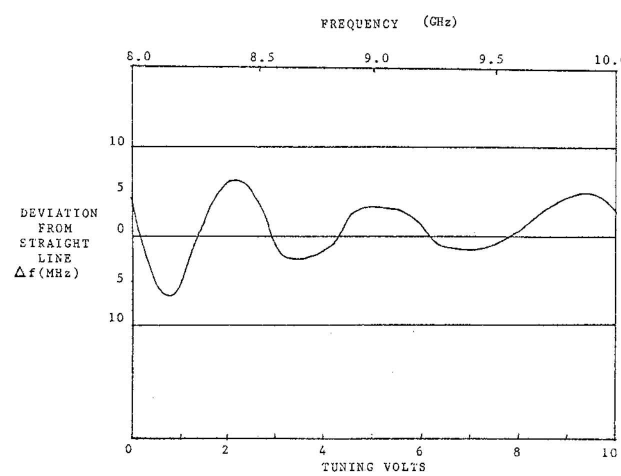

FIG. 5 LINEARITY CURVE